

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	22997	"708"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:16
L2	759	booth and 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:16
L3	367	(encoder\$3 or decoder\$3) and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:17
L4	304	3 and (partial adj product\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:17
L5	209	4 and (mux or multiplexer\$1 or multiplexor\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 15:16
L6	183	5 and (complement\$3 or invert\$3 or inversion)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:18
L7	141	6 and ((multiplier\$1 or multiplication or multiplying or multiplies).ti. or (multiplier\$1 or multiplication or multiplying or multiplies).clm. or (multiplier\$1 or multiplication or multiplying or multiplies).ab.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:19
L8	94	7 and delay\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:19
L9	44	8 and transistor\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 15:15

L10	75840	Kenneth.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:20
L11	1	10 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:20
L12	151	10 and 1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:20
L13	6	10 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 14:20
L14	93	708/620-714.ccls. and (booth adj encoder\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 15:15
L15	85	14 and (mux or multiplexer\$1 or select\$3 or multiplexor\$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 15:16
L16	72	15 not 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 15:16
L17	59	16 and (complement\$3 or negative)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 15:17
L18	42	17 and delay\$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/09 15:17

SEARCH HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore
Full Text Provided by the U.S. Patent and Trademark Office

Welcome
United States Patent and Trademark
Office

IEEE Xplore®
1 Million Documents
1 Million Users

Help FAQ Terms IEEE Peer Review Quick Links

Your search matched **1 of 1099723** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.
booth encoder <and> (complement <or> negative) Check to search within this result set

Results Key:
JNL = Journal or Magazine CNF = Conference STD = Standard

1 Design and Implementation of a 16 by 16 low-power two's complement multiplier
Goldovsky, A.; Patel, B.; Schulte, M.; Kolagotla, R.; Srinivas, H.; Burns, G.; Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on, Volume: 5, 28-31 May 2000
Pages:345 - 348 vol.5

[Abstract] [PDF Full-Text (348 KB)] IEEE CNF

Print Version

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ | Terms | Back to Top

Copyright © 2004 IEEE — All rights reserved

SEARCH HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs



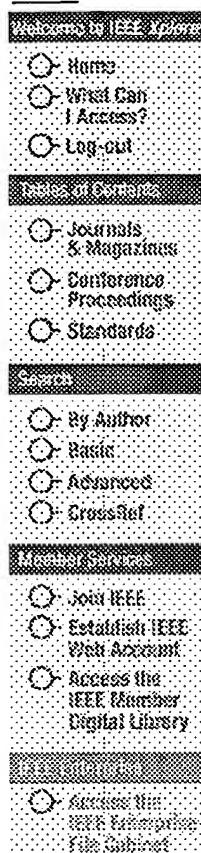
Welcome
United States Patent and Trademark
Office



Help FAQ Terms IEEE Peer Review

Quick Links

» Search Results



Your search matched **4** of **1099723** documents.

A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or entering a new one in the text box.

booth encoder <and> partial product

Check to search within this result set

Results Key:

JNL = Journal or Magazine CNF = Conference STD = Standard

1 Improved design for parallel multiplier based on phase-mode logic

Horima, Y.; Onomi, T.; Kobori, M.; Shimizu, I.; Nakajima, K.;
Applied Superconductivity, IEEE Transactions on, Volume: 13, Issue: 2
, June 2003
Pages:527 - 530

[\[Abstract\]](#) [\[PDF Full-Text \(493 KB\)\]](#) [IEEE JNL](#)

2 Design and implementation of a 16 by 16 low-power two's complement multiplier

Goldovsky, A.; Patel, B.; Schulte, M.; Kolagotla, R.; Srinivas, H.; Burns, G.;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000
IEEE International Symposium on, Volume: 5, 28-31 May 2000
Pages:345 - 348 vol.5

[\[Abstract\]](#) [\[PDF Full-Text \(348 KB\)\]](#) [IEEE CNF](#)

3 Minimizing energy dissipation in high-speed multipliers

Fried, R.;
Low Power Electronics and Design, 1997. Proceedings., 1997 International
Symposium on, 18-20 Aug. 1997
Pages:214 - 219

[\[Abstract\]](#) [\[PDF Full-Text \(420 KB\)\]](#) [IEEE CNF](#)

4 An 18 ns 56-bit multiply-adder circuit

Montoye, R.K.; Cook, P.W.; Hokenek, E.; Havreluk, R.P.;
Solid-State Circuits Conference, 1990. Digest of Technical Papers. 37th
ISSCC, 1990 IEEE International, 14-16 Feb. 1990
Pages:46 - 47, 262

[\[Abstract\]](#) [\[PDF Full-Text \(600 KB\)\]](#) [IEEE CNF](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore®
XPLORER
SEARCHED BY SUBJECT

Welcome
United States Patent and Trademark
Office

Help FAQ Terms IEEE Peer Review Quick Links

» Search Results

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.
booth <and> complement Check to search within this result set

Results Key:
JNL = Journal or Magazine CNF = Conference STD = Standard

1 Modified Booth 1's complement and modulo 2^n-1 multipliers
Efstathiou, C.; Vergos, H.T.;
Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE International Conference on, Volume: 2, 17-20 Dec. 2000
Pages:637 - 640 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(336 KB\)\]](#) **IEEE CNF**

2 On the effectiveness of residue code checking for parallel two's complement multipliers
Sparmann, U.; Reddy, S.M.;
Fault-Tolerant Computing, 1994. FTCS-24. Digest of Papers., Twenty-Fourth International Symposium on, 15-17 June 1994
Pages:219 - 228

[\[Abstract\]](#) [\[PDF Full-Text \(784 KB\)\]](#) **IEEE CNF**

3 Parallel architecture modified Booth multiplier
Cooper, A.R.;
Circuits, Devices and Systems, IEE Proceedings G [see also IEE Proceedings-Circuits, Devices, and Systems], Volume: 135, Issue: 3, June 1988
Pages:125 - 128

[\[Abstract\]](#) [\[PDF Full-Text \(316 KB\)\]](#) **IEE JNL**

4 A new architecture for 2's complement Gray encoded array multiplier
Costa, E.; Bampi, S.; Monteiro, J.;
Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium on, 9-14 Sept. 2002
Pages:14 - 19

[\[Abstract\]](#) [\[PDF Full-Text \(291 KB\)\]](#) **IEEE CNF**

5 A novel redundant binary signed-digit (RBSD) Booth's encoding
Besli, N.; Deshmukh, R.G.;
SoutheastCon, 2002. Proceedings IEEE, 5-7 April 2002
Pages:426 - 431

[\[Abstract\]](#) [\[PDF Full-Text \(496 KB\)\]](#) **IEEE CNF**

IEEE Xplore®
XPLORER
SEARCHED BY SUBJECT

Help FAQ Terms IEEE Peer Review Quick Links

» Search Results

6 Minimization of switching activities of partial products for designing low-power multipliers

Chen, O.T.-C.; Sandy Wang; Yi-Wen Wu;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, Volume: 11, Issue: 3, June 2003
Pages:418 - 433

[\[Abstract\]](#) [\[PDF Full-Text \(1277 KB\)\]](#) [IEEE JNL](#)

7 Two's complement computation sharing multiplier and its applications to high performance DFE

Hunsoo Choo; Muhammad, K.; Roy, K.;
Signal Processing, IEEE Transactions on [see also Acoustics, Speech, and Signal Processing, IEEE Transactions on], Volume: 51, Issue: 2, Feb. 2003
Pages:458 - 469

[\[Abstract\]](#) [\[PDF Full-Text \(663 KB\)\]](#) [IEEE JNL](#)

8 Approximating elementary functions with symmetric bipartite tables

Schulte, M.J.; Stine, J.E.;
Computers, IEEE Transactions on, Volume: 48, Issue: 8, Aug. 1999
Pages:842 - 847

[\[Abstract\]](#) [\[PDF Full-Text \(196 KB\)\]](#) [IEEE JNL](#)

9 On the effectiveness of residue code checking for parallel two's complement multipliers

Sparmann, U.; Reddy, S.M.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, Volume: 4, Issue: 2, June 1996
Pages:227 - 239

[\[Abstract\]](#) [\[PDF Full-Text \(1280 KB\)\]](#) [IEEE JNL](#)

10 A versatile signed array multiplier suitable for VLSI implementation

Qi Wang; Shayan, Y.R.;
Electrical and Computer Engineering, 2003. IEEE CCECE 2003. Canadian Conference on, Volume: 1, 4-7 May 2003
Pages:199 - 202 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(287 KB\)\]](#) [IEEE CNF](#)

11 Low-power multipliers by minimizing inter-data switching activities

Sandy Wang; Yi-Wen Wu; Chen, O.T.-C.; Ruey-Liang Ma;
Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on, Volume: 1, 8-11 Aug. 2000
Pages:88 - 92 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(360 KB\)\]](#) [IEEE CNF](#)

12 Design and implementation of a 16 by 16 low-power two's complement multiplier

Goldovsky, A.; Patel, B.; Schulte, M.; Kolagotla, R.; Srinivas, H.; Burns, G.;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on, Volume: 5, 28-31 May 2000
Pages:345 - 348 vol.5

[\[Abstract\]](#) [\[PDF Full-Text \(348 KB\)\]](#) [IEEE CNF](#)

13 Design of self-timed asynchronous Both's multiplier

Tin-Yau Tang; Chiu-Sing Choy; Pui-Lam Siu; Cheon-Fat Chan;
Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific, 25-28 Jan. 2000

Pages:15 - 16

[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) [IEEE CNF](#)

14 Symmetric bipartite tables for accurate function approximation

Schulte, M.J.; Stine, J.E.;

Computer Arithmetic, 1997. Proceedings., 13th IEEE Symposium on, 6-9 July 1997

Pages:175 - 183

[\[Abstract\]](#) [\[PDF Full-Text \(676 KB\)\]](#) [IEEE CNF](#)

15 A novel approach to the design and hardware implementation of high-speed digit-serial modified-Booth digital multipliers

Rao, V.M.; Nowrouzian, B.;

Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on, Volume: 3, 9-12 June 1997

Pages:1952 - 1955 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(396 KB\)\]](#) [IEEE CNF](#)

[1](#) [2](#) [3](#) [Next](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore®
1 Million Documents
1 Million Users

Welcome
United States Patent and Trademark Office

Help FAQ Terms IEEE Peer Review Quick Links

» Search Results

Your search matched **0** of **1099723** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** in **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or entering a new one in the text box.

 Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

Log-in IEEE
 Establish IEEE Web Account
 Access the IEEE Member Digital Library
 Access the IEEE Information File Library

Print Format

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved